MR-MOD

ETHERNET MEDIA RENDERER MODULE

DATASHEET

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MR-MOD-DS
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Preface

I. About This Datasheet

This document provides the information needed to design and integrate the MR-MOD Ethernet Media Renderer Module into your product. For more information, please refer to the product description available from the engineered Web site at: www.engineered.ch

II. Company Information

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If you have questions regarding the input range, please contact engineered SA customer support prior to connecting the power supply. Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the product. Please consult the datasheet prior to connecting any load. If you have doubts concerning the load specification, please contact engineered SA customer support.

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Routine maintenance is not required. This product is warranted to be free of any defect with respect to performance, quality, reliability and workmanship for a period of SIX (6) months from the date of shipment from engineered.

In the event that your product proves to be defective in any way during this warranty period, we will gladly repair or replace this piece of equipment with a unit of equal or superior performance characteristics.

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VI. Documentation Release Notice

This document is under revision control and updates will only be issued as a replacement document with a new version number.

Product specifications are subject to change without notice.

1 Introduction

1.1 Highlights

The Ethernet Media Renderer Module (MR-MOD) is a compact, easy-to-integrate OEM solution for network audio playback systems. Key features for the MR-MOD include:

- Digital Media Renderer.
- UPnP AV 2.0 / DLNA.
- Playing and decoding common audio formats* from HTTP streams.
- PCM resolution up to 32-bit, sampling rate up to 384kHz.
- Support for native DSD64, DSD128 and DSD256.
- Bit-perfect data transmission.
- 2-channel asynchronous endpoint for jitter-free stereo playback.
- Support for gapless playback.
- Embedded 32-bit digital volume attenuator.
- I2S serial audio output in slave mode.
- Ethernet RJ45 interface.
- Hardware mode for easy integration.
- SPI interface.
- Based on Analog Device Blackfin BF537 DSP.

(*) Subject to licensing by the final product manufacturer for the various audio decoders.

The MR-MOD plays music from streams, from a file server or an Internet radio, acting as a UPnP AV/DLNA Media Renderer device. Common PCM (Pulse Code Modulation) audio formats are supported, including lossless FLAC at 192kHz 24-bit. One-bit DSD (Direct Stream Digital) is also supported via uncompressed DSF and DFF files.

The Ethernet stream is asynchronous and the audio data are extracted at the rate of the local clocks. Thus, for optimal performances, the digital audio output port of the MR-MOD works in slave mode and assures bit-perfect data transfer and jitter-free clocking.

1.2 Firmware Version

This datasheet is based on the current firmware version v1.50.

1.3 Functional Block Diagram

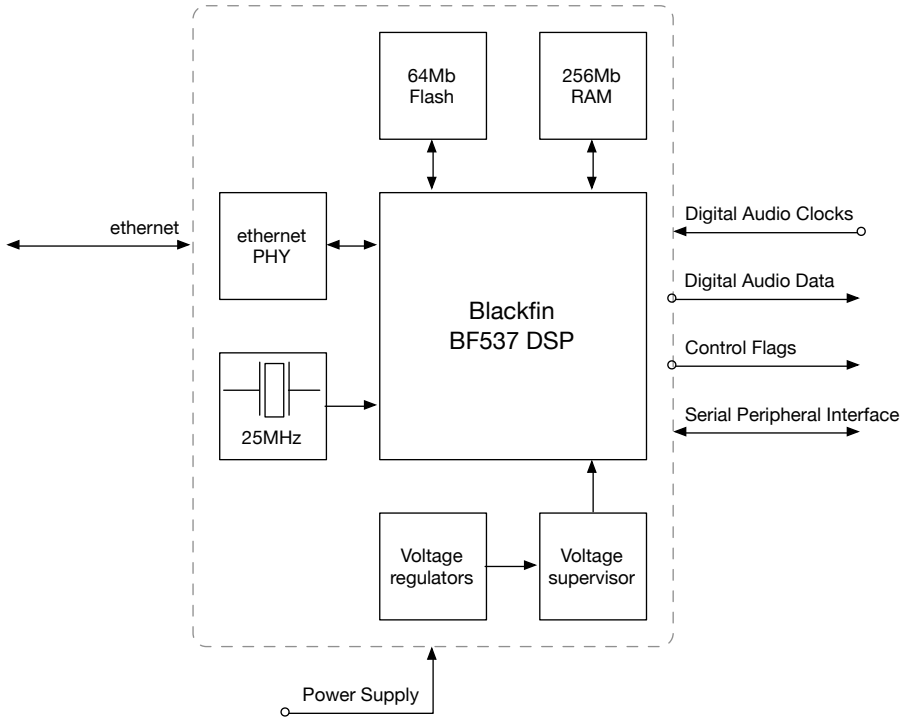

Figure 1-1 – functional block diagram

Refer to chapter 3 “Application Information” for more details about the typical setup for music playback over a home network and the MR-MOD integration.

2 Characteristics and Specifications

2.1 Electrostatic Discharge Warning

Many of the components in this product are subject to be damaged by electrostatic discharge (ESD). Customers are advised to observe proper ESD precautions when unpacking and handling the board, including the use of a grounded wrist strap at an approved ESD workstation.

Caution: Failure to observe ESD handling procedures may result in damage to the product.

2.2 Recommended Operating Conditions

Table 2-1 indicates the recommended conditions under which the product should run properly.

Parameter	Recommend Condition	
Power supply voltage	3.30V DC	
Input signal voltage	$V_{IL\ (min/max)}$: 0.0V / 0.4V	$V_{IH\ (min/max)}$: 2.4V / 3.3V
Operating free-air temperature	$T_{A(min/max)}$: 0°C / 60°C	

Table 2-1 – recommended operating conditions

2.3 Absolute Maximum Ratings

The user should be aware of the absolute maximum operating conditions for the MR-MOD. Stress beyond maximum ratings may cause permanent damage to the device. Table 2-2 summarizes the critical data points.

Parameter	Min.	Max.
Power supply voltage	-0.30V	3.60V
Input signal voltage	-0.30V	3.60V

Table 2-2 – absolute maximum ratings

2.4 Electrical Specifications

Parameter	Min.	Typ.	Max.
External DC supply voltage	3.15V	3.30V	3.45V
External DC supply current		450mA	750mA
LVTTL output high level V_{IH}	V_{DD} - 0.4V	3.10V	V_{DD}
LVTTL output low level V_{IL}	0	0.2V	0.4V

Table 2-3 – electrical specifications

2.5 Digital Audio Specifications

Parameter	Min.	Typ.	Max.
PCM input resolution	16-bit		32-bit
PCM input sampling frequency	44.1kHz		384kHz
PCM dynamic range		32-bit	
DSD input sampling frequency	2.8224MHz		11.2896MHz

Table 2-4 – digital audio specifications

2.6 Audio Formats

The following audio formats are supported by the MR-MOD:

- FLAC (Free Lossless Audio Codec)
- WAV (Waveform Audio File Format)
- MP3 (Mpeg Audio Layer 3)
- ALAC (Apple Lossless Audio Codec)
- AAC (Advanced Audio Coding)
- AIFF (Audio Interchange File Format)
- DSF and DFF (DSD stream file)

The audio data in WAV and standard AIFF files are uncompressed pulse-code modulation (PCM). Like any non-compressed, lossless format, it uses much more disk space than compressed formats. Such uncompressed PCM streams are supported up to 384kHz / 32-bit.

FLAC is an open format with royalty-free licensing. It supports for metadata tagging, album cover art, and fast seeking. The technical strengths of FLAC compared to other lossless formats lie in its ability to be streamed and decoded quickly, which is independent of compression level. Since FLAC is a lossless scheme, it is suitable as an archive format for owners of CDs and other media who wish to preserve their audio collections. The MR-MOD decodes FLAC files up to 192kHz.

MP3 and AAC are lossy compressions and encoding schemes for digital audio. These are non-free codecs covered by patents and subject to licensing by the final product manufacturer. The MR-MOD offers the technical ability to decode such formats, but engineered is not responsible for non-free audio codecs licensing.

DSF and DFF files may contain multi-channel audio data and various resolutions. The MR-MOD supports uncompressed one-bit stereo audio at 2.8224MHz, 5.6448MHz and 11.2896MHz.

Note: It is the responsibility of the manufacturer of the final product (the brand) to take care of the licensing and fees for the non-free audio codecs.

2.7 Pin Configuration

The MR-MOD uses Hirose FX8-60P-SV connectors below the board. For physical location of the pins, refer to chapter “Mechanical Data”.

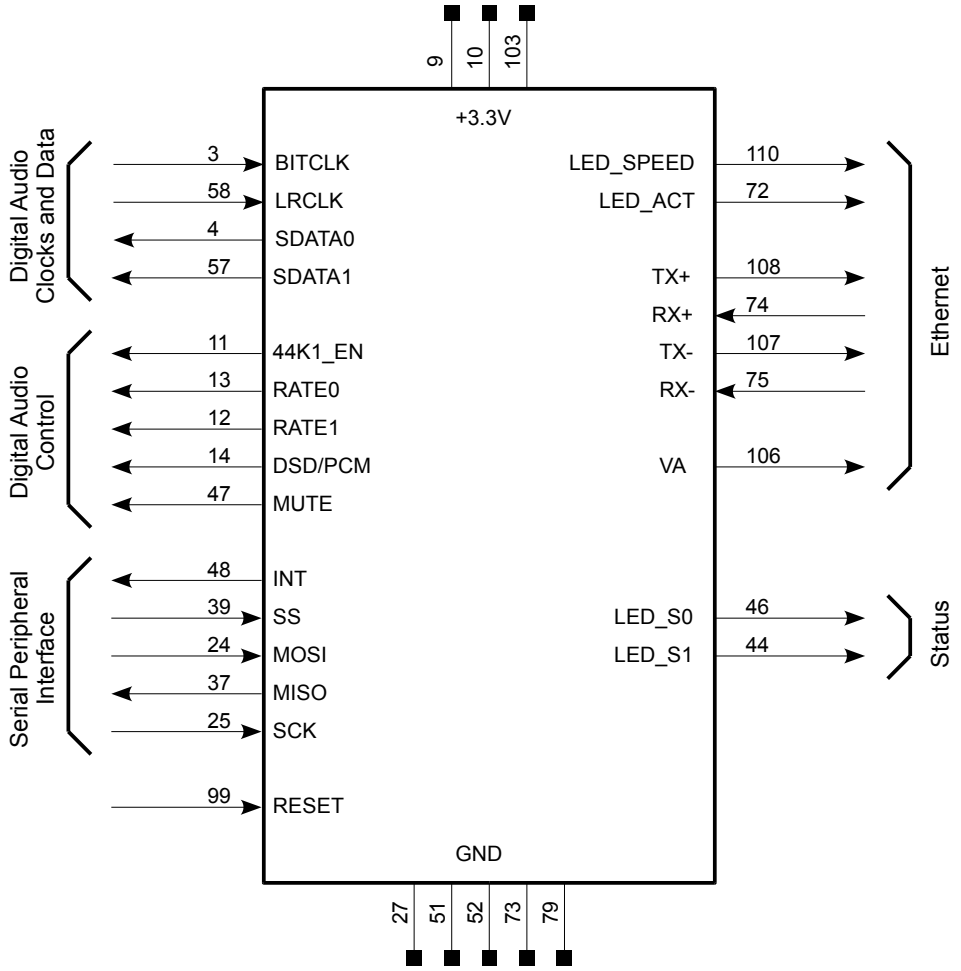

Figure 2-1 – pin configuration

2.8 Pin Descriptions

Table 2-5 describes signals and pin assignments. Pins not listed here are reserved for future use and must be left unconnected.

Pin #	Name	Type	Description
3	I2S_BITCLK	Input	Serial Audio Bit Clock Input – Serial bit clock for audio data.
58	I2S_LRCLK	Input	Serial Audio Left/Right Clock Input – Frame sync clock for PCM audio data.
4	I2S_SDATA0	Output	Serial Audio Data Output – Stereo PCM audio data or DSD audio left-channel data.
57	I2S_SDATA1	Output	Serial Audio Data Output – DSD audio right-channel data.
11	CC_44K1_EN	Output	Sampling Frequency Low: the sampling frequency is a multiple of 44.1kHz. High: the sampling frequency is a multiple of 48kHz. Refer to Table 3-1.
12	CC_RATE1	Output	Sampling Rate Flag – Sampling rate information. Refer to Table 3-1.
13	CC_RATE0	Output	Sampling Rate Flag – Sampling rate information. Refer to Table 3-1.
47	CC_MUTE	Output	Mute Low: the audio data stream is not valid and the DAC must be muted. High: the audio data stream is valid.
14	CC_DSD/PCM	Output	DSD Format Low: the output signal is PCM High: the output signal is DSD
48	SPI_INT	Output	SPI Interrupt – Active low.
39	SPI_SS	Input	SPI Slave Select – Active low.
24	SPI_MOSI	Input	SPI Data Input
37	SPI_MISO	Output	SPI Data Output
25	SPI_SCK	Input	SPI Clock
46	LED_S0	Output	Status LED 0 – Active high.
44	LED_S1	Output	Status LED 1 – Active high.
72	ETH_LED_ACT	Output	Ethernet Activity LED – Active low, blink on activity.
74	ETH_RX+	Output	Ethernet
75	ETH_RX-	Output	Ethernet
106	ETH_VA	Power	Ethernet – Power.
108	ETH_TX+	Output	Ethernet
107	ETH_TX-	Output	Ethernet
110	ETH_LED_SPEED	Output	Ethernet Speed LED – Indicates selected speed 10/100. 0: 100Mb / 1: 10Mb.
99	RESET#	Input	Reset – Active low. This signal may be used to force a reset. If not used, do not connect.
9	VDD	Power	Power Supply Input: +3.30V
10	VDD	Power	Power Supply Input: +3.30V
103	VDD	Power	Power Supply Input: +3.30V
27	GND	Ground	Ground
51	GND	Ground	Ground
52	GND	Ground	Ground
73	GND	Ground	Ground
79	GND	Ground	Ground

Table 2-5 – pin descriptions

3 Application Information

3.1 Home Network Devices

3.1.1 Digital Media Server (DMS)

Multimedia files are stored on this device and are made available to the network Digital Media Renderers.
Ex. : computer, network-attached storage (NAS) devices.

3.1.2 Digital Media Renderer (DMR)

This device is controlled by a Digital Control Point and can play the content of a Digital Media Server.
Ex. : network audio player based on the MR-MOD, audio/video receiver, TV, remote speakers.

3.1.3 Digital Control Point (DCP)

This device can browse the content on a Digital Media Server and control a Digital Media Renderer to play these files.
Ex. : smartphone, tablet, computer.

3.2 Typical Setup

The MR-MOD provides a very high quality solution to play audio files on a home network. Thanks to its compatibility with the UPnP AV 2.0 standard, its integration into a home network is very easy.
Developed for high-end Hi-Fi systems, it achieves bit-perfect playback with no compromise on sound quality.

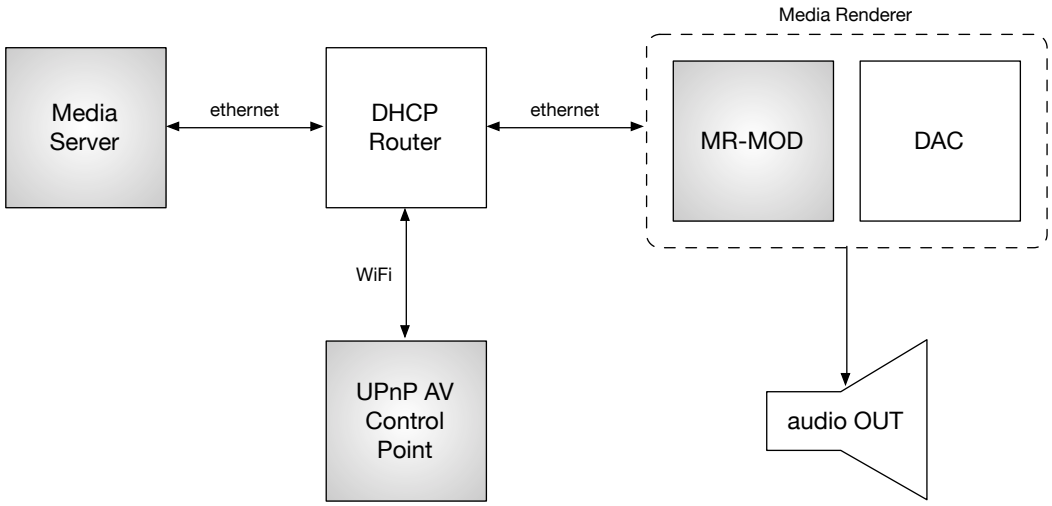

Figure 3-1 – typical setup of a network audio system

How it works:

1. Music files are stored on the Media Server.
2. The user can browse the files and send/receive commands (play, volume, display time, cover...) via the Control Point.
3. The network audio Media Renderer Module (MR-MOD) fetches a stream to play from the Media Server, then converts it into audio data.
4. The audio data are sent to the DAC which converts them into an analog signal. This signal can then be amplified and played on speakers.

3.3 Typical Application

The designer has several options to integrate the MR-MOD OEM module into a system. For instance, the I2S serial audio data output bus can be connected to:

- a D/A Converter (DAC) in order to output analog audio signal
- a Digital audio Transmitter (DIT) in order to output S/PDIF signal
- a DSP to apply digital processing (e.g. oversampling)
- an FPGA for clock and signal routing

The I2S output port of the module is configured as a slave device. Bit clock and left/right clock have to be provided by an external device, being a D/A converter, an FPGA or any other circuit able to be clock master on the digital audio bus.

However, bit clock and left/right clock frequency have to match the sampling rate of the file played over the network, which involves the following concept:

- generating two master clocks: 22.5792MHz and 24.5760MHz
- selecting the appropriate master clock by reading the hardware flag 44K1_EN#
- dividing the master clock by the appropriate ratio to produce bit clock and left/right clock, according to the hardware flags RATE0 and RATE1

The behaviour of the hardware flags in explained further in Table 3-1. Clock frequencies and ratios are detailed in Table 3-2.

The following drawing illustrates an application where the clock selection, DAC and DIT configuration is performed by a micro-controller (MCU).

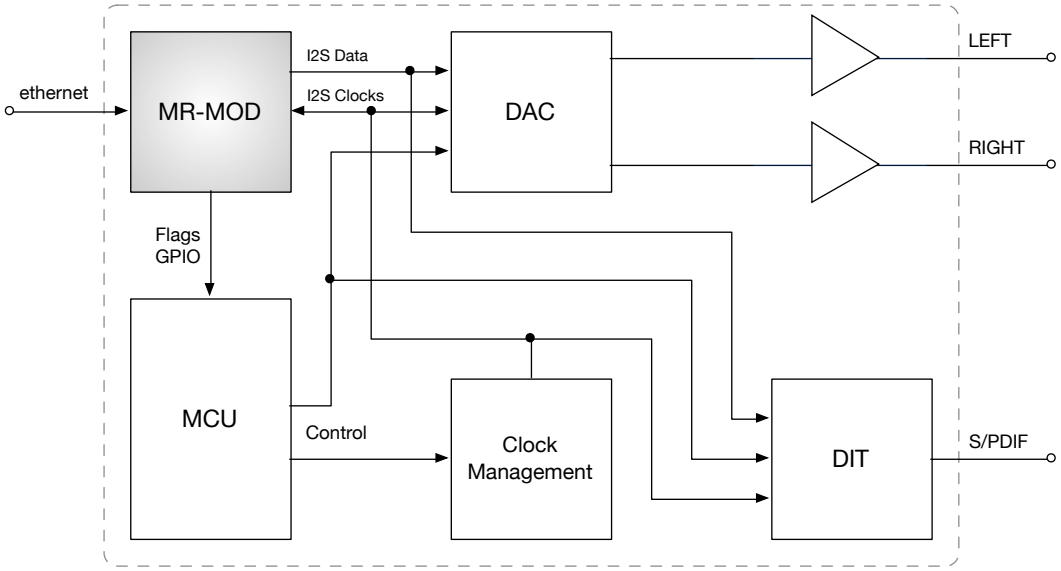

Figure 3-2 – example of a network audio player based on the MR-MOD

3.4 Power Supply

The MR-MOD module integrates a voltage supervisor that resets the DSP when the power supply drops below a defined threshold. Power supply regulation, voltage precision, current capability and connexion impedance are important factors to ensure clean operation of the module.

Caution: Failure to respect the power supply polarity and voltage level may result in damage to the product.

3.5 Clock Management

The MR-MOD I2S port is clock-slave. Master clock, bit clock and left/right clock (MCLK, BITCLK, LRCLK) must be supplied externally, as shown in Figure 3-3.

An external logic has to monitor the hardware flags (RATE0, RATE1 and 44K1_EN#) and select the correct clocks to driver the MR-MOD I2S port. See Table 3-1 and Table 3-2 for more information.

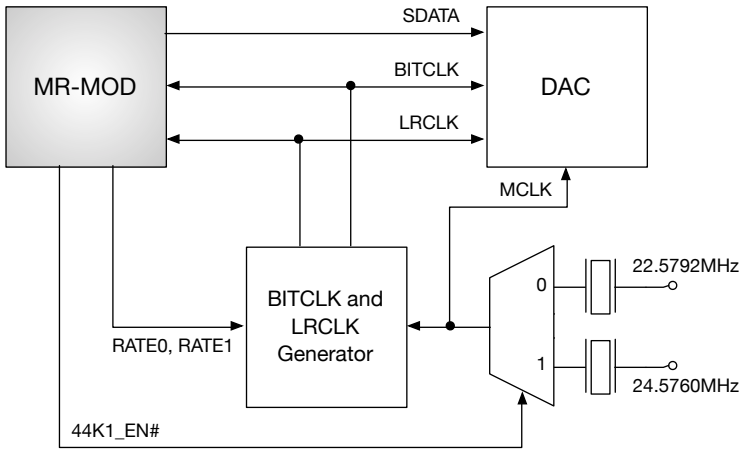

Figure 3-3 – clock management

3.6 I2S Digital Audio Bus

The digital audio port is configured in I2S, slave mode. Bit and left/right clocks are generated externally. The MR-MOD supplies the data signals and the clock management information.

The data signals are made of two lines: SDATA0 and SDATA1. By default, only SDATA0 is used in PCM audio.

The clock management information is made of three signals: RATE0, RATE1 and $\overline{44K1\_EN}$ (Table 3-1).

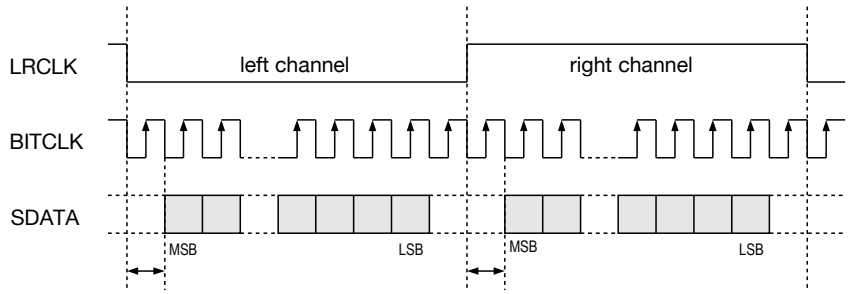

Figure 3-4 – I2S data format

The MUTE signal indicates whenever the serial data are no longer valid and therefore should be discarded.

Table 3-1 shows how the clock mode signals must be decoded.

Left/Right Clock Frequency (Fs)	RATE0	RATE1	44K1_EN
44.1kHz	High	High	Low
48kHz	High	High	High
88.2kHz	Low	High	Low
96kHz	Low	High	High
176.4kHz	High	Low	Low
192kHz	High	Low	High
352.8kHz	Low	Low	Low
384kHz	Low	Low	High

Table 3-1 – relation between sampling frequency and hardware flags

Table 3-2 shows how the audio sampling frequency (Fs), the bit clock frequency and the master clock frequency are related.

Left/Right Clock Frequency (Fs)	Bit Clock Ratio	Master Clock Ratio	Master Clock Frequency
44.1kHz	64 * Fs	512 * Fs	22.5792MHz
48kHz	64 * Fs	512 * Fs	24.5760MHz
88.2kHz	64 * Fs	256 * Fs	22.5792MHz
96kHz	64 * Fs	256 * Fs	24.5760MHz
176.4kHz	64 * Fs	128 * Fs	22.5792MHz
192kHz	64 * Fs	128 * Fs	24.5760MHz
352.8kHz	64 * Fs	64 * Fs	22.5792MHz
384kHz	64 * Fs	64 * Fs	24.5760MHz

Table 3-2 – relation between left/right clock, master clock and bit clock

3.7 DSD Mode

When playing DSD, the I2S digital audio bus is re-configured in order to output DSD data. Left/right clock (LRCLK) is discarded.

Pin #	Name	PCM Signal	DSD Signal
3	I2S_BITCLK	BITCLK	BITCLK
58	I2S_LRCLK	LRCLK	n/a
4	I2S_SDATA0	PCM data L/R	DSD data left
57	I2S_SDATA1	n/a	DSD data right
14	CC_DSD/PCM	Low	High

Table 3-3 – pin mapping in PCM and DSD mode

Support for native DSD64, DSD128 as well as DSD256 is provided by the MR-MOD module. DSD data format is indicated by the flag CC_DSD/PCM on pin 14.

CC_DSD/PCM	Data Stream Type
Low	PCM
High	DSD

Table 3-4 – Data stream type

Table 3-5 shows how the DSD frequency is indicated by the hardware flags, and Table 3-6 illustrates the relation between DSD rate, Bit Clock and Master Clock frequencies.

DSD Type	RATE0	RATE1	44K1_EN#
DSD 64	High	High	Low
DSD 128	Low	High	Low
DSD 256	High	Low	Low

Table 3-5 – Relation between DSD rate and hardware flags

DSD Type	Bit Clock Frequency	Master Clock Frequency
DSD 64	2.8224MHz	22.5792MHz
DSD 128	5.6448MHz	22.5792MHz
DSD 256	11.2896MHz	22.5792MHz

Table 3-6 – Relation between DSD rate, bit clock and master clock

3.8 Ethernet Interfacing

The MR-MOD integrates an on-board Ethernet interface. Only the RJ45 connector and ESD protection are needed on the backplane board, as shown on Figure 3-5.

Note: RJ45 connector is shown here for reference only, and based on part number J0011D01NL from Pulse Electronics Corporation. Pin numbering varies from one manufacturer/model to the other.

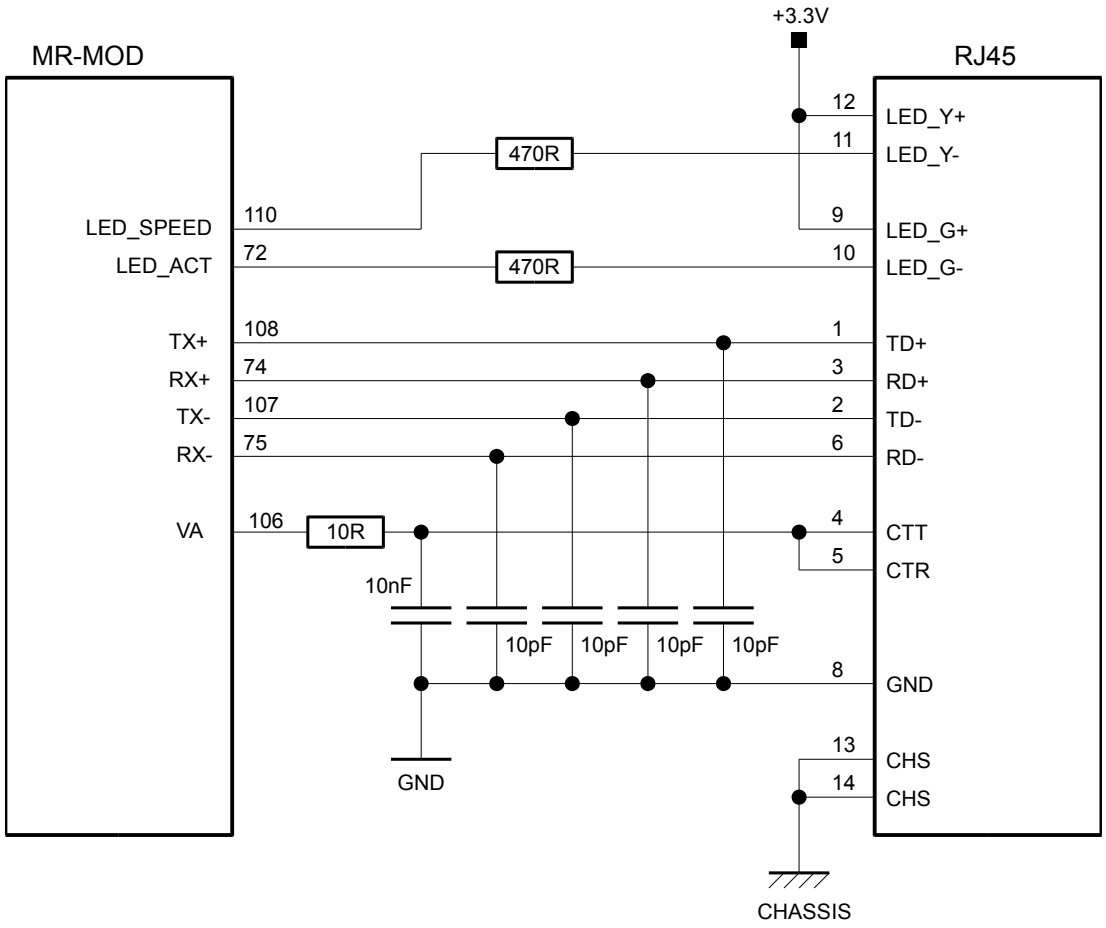

Figure 3-5 – Ethernet interfacing

3.9 Network Setup

The MR-MOD is compatible with the UPnP AV/DLNA specification and no specific user configuration is needed to integrate it into an Ethernet network. There must be a DHCP server on the network where the MR-MOD operates. The MR-MOD will fetch its configuration information directly from the DHCP server.

Two status signals give information about the boot status of the module. They can be connected to status LEDs for diagnostic.

LED_S1	LED_S0	Description
1	1	Power up. Booting.
1	0	System booted
0	1	System booted. Network configured.
0	0	An error occurred

Table 3-7 – status LED description

3.10 Digital Volume Control

The volume information is transmitted from the Control Point to the MR-MOD via the Ethernet connection. By default, the corresponding attenuation is then computed inside the DSP and applied to the serial audio data output.

Most of basic digital volume controllers deteriorate the audio signal due to truncation or rounding errors, but thanks to a 32-bit calculation the signal integrity is preserved here.

Please note that there is a latency on volume changes due to the renderer's buffering system.

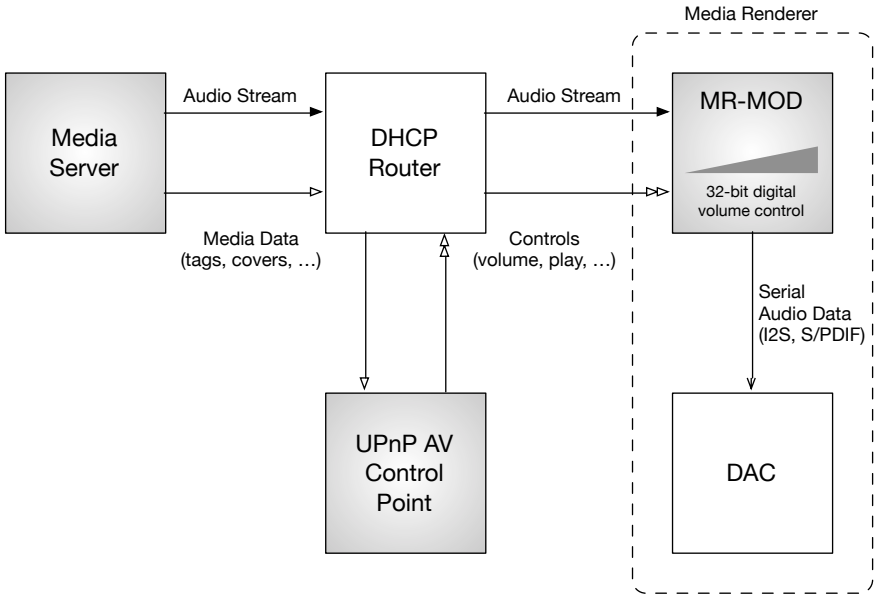

Figure 3-6 – volume control description

The MR-MOD embedded volume control can be disabled via the SPI interface. In this case, the attenuation is not applied on the data and the volume control information is available for reading via SPI. Refer to chapter 4 “Serial Peripheral Interface (SPI)” for more information.

4 Serial Peripheral Interface (SPI)

The MR-MOD features a full-duplex serial port based on the Serial Peripheral Interface standard.

The SPI port communicates in slave mode. It is used to access registers allowing the MR-MOD module to transmit information to the host device, referred as master, and to be configured for the desired operational mode. An interrupt line is provided to indicate a data change and avoid the need for the host to poll the MR-MOD continuously. The operation of the SPI port may be completely asynchronous with respect to the audio stream rates.

4.1 Register interface

The SPI port is a five-wires serial interface where SPI_SS (active low) is the module chip select signal, SPI_SCK is the control port bit clock (input into the MR-MOD from the host device), SPI_MOSI is the input data line from master, SPI_MISO is the output data line to the master and SPI_INT is the interrupt line.

Data words are 16-bit long and transmitted in MSBF format. Data is clocked in on the rising edge of SPI_SCK and clocked out on the falling edge.

Figure 4-1 and Figure 4-2 illustrate the operation of the SPI port as well as the protocol for register read and write operations.

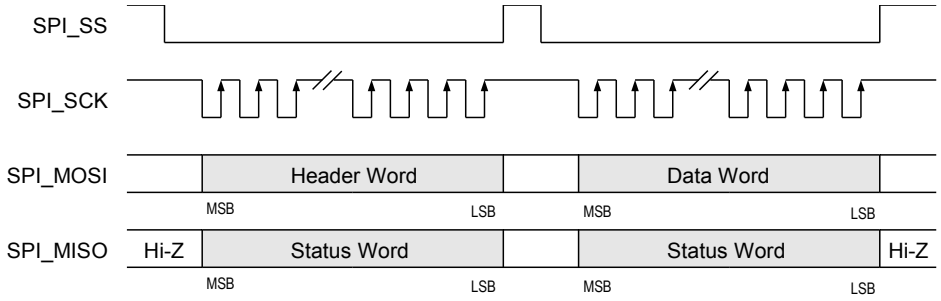

Figure 4-1 – SPI protocol for register write operation

The register WRITE operation requires two 16-bit words to be sent by the host device. A handshaking mechanism ensures that the transfer is valid. Refer to the register description hereafter for detailed information.

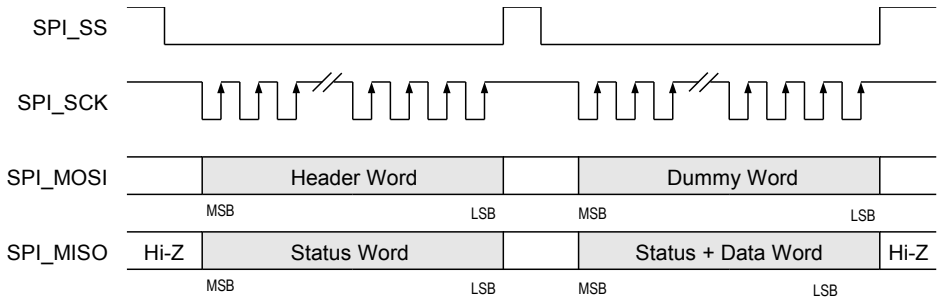

Figure 4-2 – SPI protocol for register read operation

The register READ operation requires two 16-bit words to be sent by the host device, the second one being a dummy word. A handshaking mechanism ensures that the transfer is valid. Refer to the register description hereafter for detailed information.

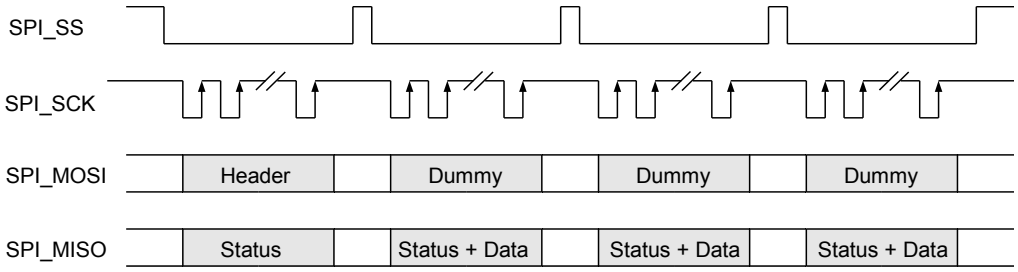

Figure 4-3 – SPI protocol for register burst read operation.

Some registers allow reading more than one word and therefore a longer data transfer is required. This happens with string and buffer data types. When accessing these registers, a burst read transfer is used. The length of the transfer depends on the data type.

A register access is made of one Header Word followed by one or more Data/Dummy Word. Delay between each Word transferred is critical, please refer to the timing specification. If the maximum delay is not respected, a timeout occur, the communication is reset and the next expected Word is a Header.

All transfers rely upon a handshaking mechanism. This handshaking mechanism uses four bits of the word transmitted by the MR-MOD to the host. The VALID bit indicates whenever the SPI transfer is valid or not, meanwhile the PARITY bit allows for parity check. The READY bit indicates if the device is ready to process the transfer or if this must be repeated. The STATE bit indicates if the current transfer is related to a Header or a Data Word.

READY bit cleared means that the DSP is not ready to process the communication. The last Word sent by the host is lost, and the reply is not valid. The last Word must be sent again by the host until READY is set.

A wrong VALID or PARITY bit means a transmission error occurred. The use must abort the transfer and wait at least the communication timeout before restarting a new transfer.

The STATE bit is here to help the user to detect a misalignment in the Header/Data sequencing. Handling of this bit is not mandatory.

The Header Word sent by the host is defined as follows:

Word Name	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Header	0	0	0	0	0	0	0	0	R/W	A6	A5	A4	A3	A2	A1	A0

Table 4-1 – header word definition

Bit 15-8 : Set to 0
Bit 7 : R/$\overline{W}$: defines a Read or Write operation
0 = Write operation
1 = Read operation
Bit 6-0 : A6-A0: register address

The Dummy Word sent by the host for a register read operation is not used. All bits must be set to zero.

The Data Word sent by the host for a register write operation is defined as follows:

Word Name	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Data	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

Table 4-2 – data word definition

Bit 15-8 : Set to 0
Bit 7-0 : Data

The Status Word sent by the MR-MOD is defined as follows:

Word Name	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Status	READY	STATE	PARITY	VALID	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-3 – status word definition

MSB : READY: ready bit
0 = device is not ready and transfer failed
1 = device is ready and transfer succeeded

Bit 14 : STATE: indicates whenever the Word received by the MR-MOD is a Header or Data
0 = DATA state
1 = CMD state

Bit 13 : PARITY: even parity in bits 15 to 0
The number of '1' in bits 15 to 0 (including the parity bit) is even

Bit 12 : VALID: valid bit
0 = transfer succeeded
1 = transfer failed

Bit 11-0 : Set to 0

The Status + Data Word sent by the MR-MOD is defined as follows:

Word Name	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Status + Data	READY	STATE	PARITY	VALID	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

Table 4-4 – status + data word definition

MSB : READY: ready bit
0 = device is not ready and transfer failed
1 = device is ready and transfer succeeded

Bit 14 : STATE: interface current status
0 = current transfer from the host is a Data/Dummy Word
1 = current transfer from the host is a Header Word

Bit 13 : PARITY: even parity in bits 15 to 0
The number of '1' in bits 15 to 0 (including the parity bit) is even

Bit 12 : VALID: valid bit
0 = transfer succeeded
1 = transfer failed

Bit 11-8 : Set to 0
Bit 7-0 : Data

4.2 Interrupts

An interrupt line is provided to indicate a data change and avoid the need for the host to poll the MR-MOD continuously. The interrupt line is an active low signal, asserted when one or more interrupt flags are set.

There are 15 active high interrupt flag bits dispatched in the three registers. Refer to registers definition for detailed information. Interrupt flag bits are set when a change occurs in the related data.

Interrupt flags must be cleared by the user software once the interrupt has been handled by the host. Writing a '0' clears the corresponding interrupt flag.

The interrupt line is deasserted when all interrupt flags are cleared.

4.3 Timing Requirements

SPI timing requirements are specified according to the following chart and diagram.

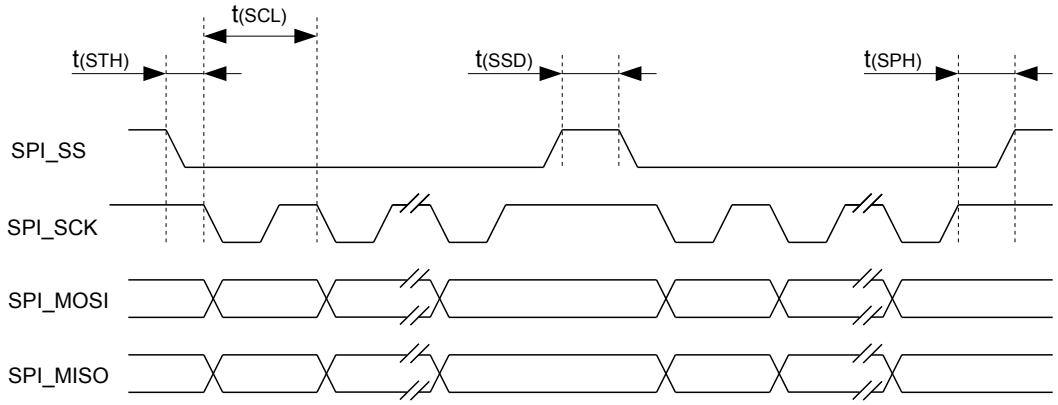

Figure 4-4 – SPI protocol timing diagram

Parameter	Description	Min	Max	Unit
f_{SCLK}	Serial Clock frequency		4	MHz
t_{SCLK}	Serial Clock period	250		ns
t_{STH}	Hold time for start condition	50		ns
t_{SSD}	Chip Select deassertion min. time	7		µs
t_{SSD}	Chip Select deassertion max. time		500	ms
t_{SPH}	Hold time for stop condition		50	ns

Table 4-5 – SPI timing requirements

4.4 Register Types

Registers are entry points to access different types of data. There are three data types: Byte, String and Buffer.

The Byte is the simplest type and is used where a single data byte is needed, for instance with status register, volume control and volume level.

The String type consists of a table of ASCII-encoded chars. As in standard C language, the last byte is a zero. When accessing a register that implements a string, burst read mode must be used and data must be read until a data zero is read. The String type is used for Artist/Album/Track Names and Track Format.

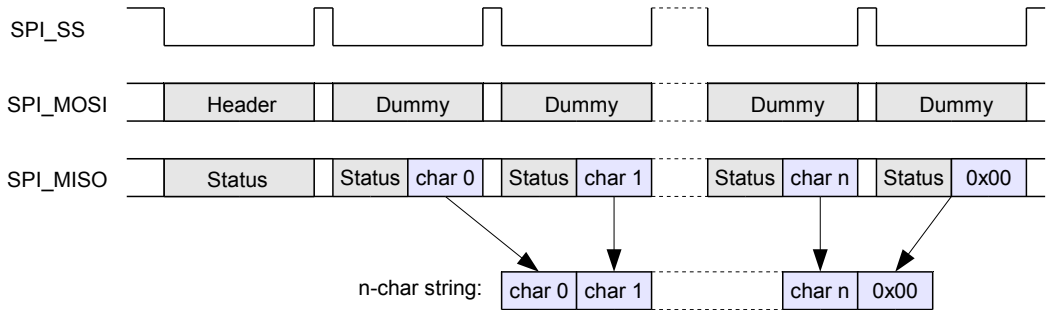

Figure 4-5 – string register read operation

The Buffer type is composed of two sections: Length and Data. Length is an unsigned integer of 4 bytes sent LSB first. It indicates the size of the Data table. When accessing a register that implements a buffer, burst read mode must be used to read the entire Data table. The Buffer type is used for the Cover.

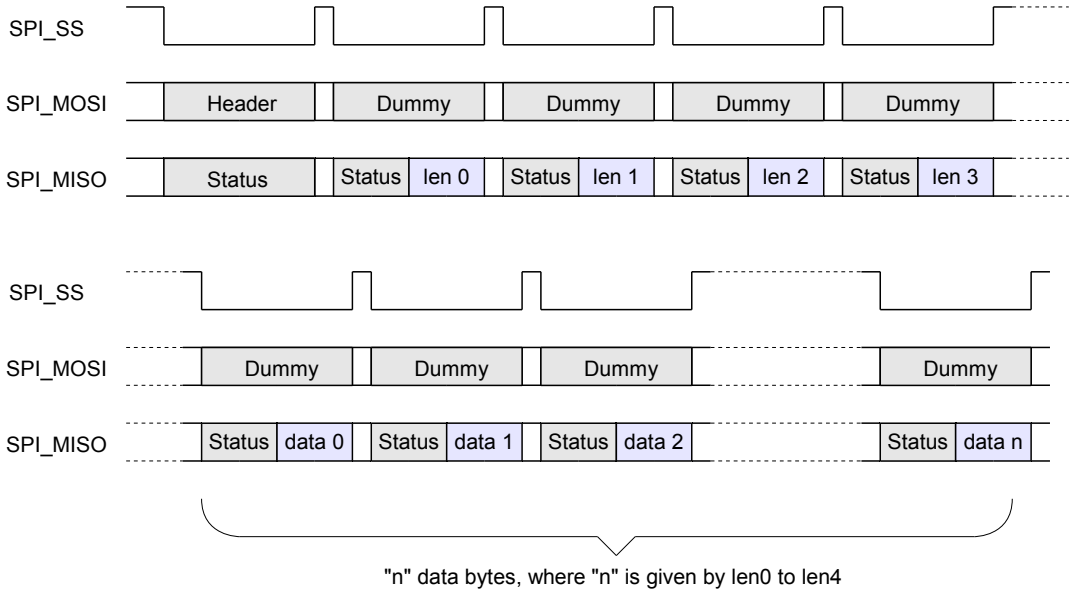

Figure 4-6 – buffer register read operation

When accessing a String or Buffer Register Type, it is important to note that the data should be read until the end. If not, a timeout condition will occur and the next access shall restart from the beginning.

4.5 Register Map

Table 4-6 summarizes the MR-MOD registers.

Addr	Name	Description	Direction	Type
0x40	VOL	Digital Volume Level	OUT	Byte
0x41	DVC	Digital Volume Control	IN	Byte
0x42	ETL	Elapsed Time LSB	OUT	Byte
0x43	ETH	Elapsed Time MSB	OUT	Byte
0x44	TDL	Track Duration LSB	OUT	Byte
0x45	TDH	Track Duration MSB	OUT	Byte
0x46	PS	Player Status	OUT	Byte
0x47	ARN	Artist Name	OUT	String
0x48	ALN	Album Name	OUT	String
0x49	TRN	Track Name	OUT	String
0x4A	COV	Cover	OUT	Buffer
0x4B	TRF	Track Format	OUT	String
0x4C	IP0	IP Address byte 0	OUT	Byte
0x4D	IP1	IP Address byte 1	OUT	Byte
0x4E	IP2	IP Address byte 2	OUT	Byte
0x4F	IP3	IP Address byte 3	OUT	Byte
0x50	IF0	Interrupt Flags register 0	OUT	Byte
0x51	IF1	Interrupt Flags register 1	OUT	Byte
0x52	IF2	Interrupt Flags register 2	OUT	Byte
0x59	OFMT	Output Format	OUT	Byte
0x60	ELS	Ethernet Link Status	OUT	Byte
0x61	SR	Sample Rate	OUT	Byte
0x62	BPS	Bit per Sample	OUT	Byte
0x65	MAG	Magic	OUT	Byte
0x66	SCR	Scratch	IN/OUT	Byte
0x68	MAC0	Ethernet MAC Address Byte 0	OUT	Byte
0x69	MAC1	Ethernet MAC Address Byte 1	OUT	Byte
0x6A	MAC2	Ethernet MAC Address Byte 2	OUT	Byte
0x6B	MAC3	Ethernet MAC Address Byte 3	OUT	Byte
0x6C	MAC4	Ethernet MAC Address Byte 4	OUT	Byte
0x6D	MAC5	Ethernet MAC Address Byte 5	OUT	Byte
0x6F	FIRM	Firmware Version	OUT	String

Table 4-6 – register map

4.6 Registers Definition

This section gives details and bits definition for each register as well as their default setting after power-up.

4.6.1 Register 0x40: VOL

Description : Digital Volume Level
Type : Byte
Details : The Volume Level is expressed in percent. This is an unsigned 8-bit integer. The volume range is 0...100. The default value is 100.

4.6.2 Register 0x41: DVC

Description : Digital Volume Control
Type : Byte
Mode : 0 = Digital Volume ON
1 = Digital Volume OFF

DVC	7	6	5	4	3	2	1	0
Bit Name	X	X	X	X	X	X	X	Mode
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

4.6.3 Register 0x42: ETL

Description : Elapsed Time LSB
Type : Byte
Details : The Elapsed Time is expressed in seconds. This is a 16-bit unsigned integer value formed by the two bytes of registers ETH and ETL.

4.6.4 Register 0x43: ETH

Description : Elapsed Time MSB
Type : Byte
Details : The Elapsed Time is expressed in seconds. This is a 16-bit unsigned integer value formed by the two bytes of registers ETH and ETL.

4.6.5 Register 0x44: TDL

Description : Track Duration LSB
Type : Byte
Details : The Track Duration is expressed in seconds. This is a 16-bit unsigned integer value formed by the two bytes of registers TDH and TDL.

4.6.6 Register 0x45: TDH

Description : Track Duration MSB
Type : Byte
Details : Track Duration is expressed in seconds. This is a 16-bit unsigned integer value formed by the two bytes of registers TDH and TDL.

4.6.7 Register 0x46: PS

Description : Player Status
Type : Byte
PS : 00 = STOPPED
01 = PLAYING
10 = PAUSED

PS	7	6	5	4	3	2	1	0
Bit Name	X	X	X	X	X	X	PS1	PS0
Access Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

4.6.8 Register 0x47: ARN

Description : Artist Name
Type : String
Details : The Artist Name is a String composed of ASCII-encoded printable characters and terminated by a null character.

4.6.9 Register 0x48: ALN

Description : Album Name
Type : String
Details : The Album Name is a String composed of ASCII-encoded printable characters and terminated by a null character.

4.6.10 Register 0x49: TRN

Description : Track Name
Type : String
Details : The Track Name is a String composed of ASCII-encoded printable characters and terminated by a null character.

4.6.11 Register 0x4A: COV

Description : Cover
Type : Buffer
Details : The Cover is actually not implemented and will return an empty buffer.

4.6.12 Register 0x4B: TRF

Description : Track Format
Type : String
Details : The Track Format is a String composed of ASCII-encoded printable characters and terminated by a null character.

4.6.13 Register 0x4C: IP0

Description : IP Address byte 0
Type : Byte
Details : The IP address is made of four IP Byte Registers to form the complete MR-MOD IP address according to the structure: IP3.IP2.IP1.IP0

4.6.14 Register 0x4D: IP1

Description : IP Address byte 1
Type : Byte
Details : The IP address is made of four IP Byte Registers to form the complete MR-MOD IP address according to the structure: IP3.IP2.IP1.IP0

4.6.15 Register 0x4E: IP2

Description : IP Address byte 2
Type : Byte
Details : The IP address is made of four IP Byte Registers to form the complete MR-MOD IP address according to the structure: IP3.IP2.IP1.IP0

4.6.16 Register 0x4F: IP3

Description : IP Address byte 3
Type : Byte
Details : The IP address is made of four IP Byte Registers to form the complete MR-MOD IP address according to the structure: IP3.IP2.IP1.IP0

4.6.17 Register 0x50: IF0

Description : Interrupt Flags Register 0
Type : Byte
VOL : Volume changed
ET : Elapsed Time changed
TD : Track Duration changed
PS : Player Status changed
ARN : Artist Name changed
ALN : Album Name changed
TRN : Track Name changed
COV : Cover changed

IF0	7	6	5	4	3	2	1	0
Bit Name	COV	TRN	ALN	ARN	PS	TD	ET	VOL
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

4.6.18 Register 0x51: IF1

Description : Interrupt Flags Register 1
Type : Byte
TRF : Track Format changed
IP : IP address changed
ELS : Ethernet Link Status changed
SR : Sample Rate changed
BPS : Bits per sample changed
MAC : MAC address changed

IF1	7	6	5	4	3	2	1	0
Bit Name	X	X	MAC	BPS	SR	ELS	IP	TRF
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Refer to section 4.2 “Interrupts” for more information about interrupt handling.

4.6.19 Register 0x52: IF2

Description : Interrupt Flags Register 2
Type : Byte
OFMT : Output Format changed

IF2	7	6	5	4	3	2	1	0
Bit Name	X	X	X	X	X	X	X	OFMT
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Refer to section 4.2 “Interrupts” for more information about interrupt handling.

4.6.20 Register 0x59: OFMT

Description : Output Format
Type : Byte
nD/P : DSD/PCM indicator
0 = output signal PCM
1 = output signal DSD

OFMT	7	6	5	4	3	2	1	0
Bit Name	X	X	X	X	X	X	X	nD/P
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

4.6.21 Register 0x60: ELS

Description : Ethernet Link Status
Type : Byte
ELS : 0 = link is down
1 = link is up

ELS	7	6	5	4	3	2	1	0
Bit Name	X	X	X	X	X	X	X	ELS
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

4.6.22 Register 0x61: SR

Description : Sample Rate
Type : Byte
SR : 0 = 44100 Hz ; 1 = 48000 Hz ; 2 = 88200 Hz ; 3 = 96000 Hz
4 = 176400 Hz ; 5 = 192000 Hz ; 6 = 352800Hz ; 7 = 384000 Hz

SR	7	6	5	4	3	2	1	0
Bit Name	X	X	X	X	X	SR2	SR1	SR0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

4.6.23 Register 0x62: BPS

Description : Bits Per Sample
Type : Byte
BPS : 0 = 16-bit sample
1 = 24-bit sample
2 = 32-bit sample

BPS	7	6	5	4	3	2	1	0
Bit Name	X	X	X	X	X	X	BPS1	BPS0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

4.6.24 Register 0x65: MAG

Description : Magic
Type : Byte
Details : The Magic register is used for debugging purpose. It always return the value 0xA5. It cannot be written.

MAG	7	6	5	4	3	2	1	0
Bit Name	MAG7	MAG6	MAG5	MAG4	MAG3	MAG2	MAG1	MAG0
Access Type	R	R	R	R	R	R	R	R
Default	1	0	1	0	0	1	0	1

4.6.25 Register 0x66: SCR

Description : Scratch
Type : Byte
Details : The Scratch register is used for debugging purpose. On read it will return the previously written value.

SCR	7	6	5	4	3	2	1	0
Bit Name	SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

4.6.26 Register 0x68: MAC0

Description : MAC Address byte 0
Type : Byte
Details : The MAC address is made of six MAC Byte Registers to form the complete MR-MOD MAC address according to the structure: MAC0:MAC1:MAC2:MAC3:MAC4:MAC5

4.6.27 Register 0x69: MAC1

Description : MAC Address byte 1
Type : Byte
Details : The MAC address is made of six MAC Byte Registers to form the complete MR-MOD MAC address according to the structure: MAC0:MAC1:MAC2:MAC3:MAC4:MAC5

4.6.28 Register 0x6A: MAC2

Description : MAC Address byte 2
Type : Byte
Details : The MAC address is made of six MAC Byte Registers to form the complete MR-MOD MAC address according to the structure: MAC0:MAC1:MAC2:MAC3:MAC4:MAC5

4.6.29 Register 0x6B: MAC3

Description : MAC Address byte 3
Type : Byte
Details : The MAC address is made of six MAC Byte Registers to form the complete MR-MOD MAC address according to the structure: MAC0:MAC1:MAC2:MAC3:MAC4:MAC5

4.6.30 Register 0x6C: MAC4

Description : MAC Address byte 4
Type : Byte
Details : The MAC address is made of six MAC Byte Registers to form the complete MR-MOD MAC address according to the structure: MAC0:MAC1:MAC2:MAC3:MAC4:MAC5

4.6.31 Register 0x6D: MAC5

Description : MAC Address byte 5
Type : Byte
Details : The MAC address is made of six MAC Byte Registers to form the complete MR-MOD MAC address according to the structure: MAC0:MAC1:MAC2:MAC3:MAC4:MAC5

4.6.32 Register 0x6F: FIRM

Description : Firmware Version
Type : String
Details : The Firmware Version is a String composed of ASCII-encoded printable characters and terminated by a null character.

5 Firmware Update

The firmware update requires a computer connected on the same network as the MR-MOD. Once the device has booted and is registered on the network, its information Web page can be accessed with an Internet browser. This page contains the firmware update interface.

On MS Windows-based computers, browsing the network gives easy access to the media renderer, displayed in the Network window under the label "Media Devices". A double-click on the "Audio Renderer-XX" icon shows the information Web page.

On other operating systems, it may be required to access the router's DHCP table to get the renderer's IP address. Then simply enter the IP address in your browser to access it.

The information page contains the firmware update interface.

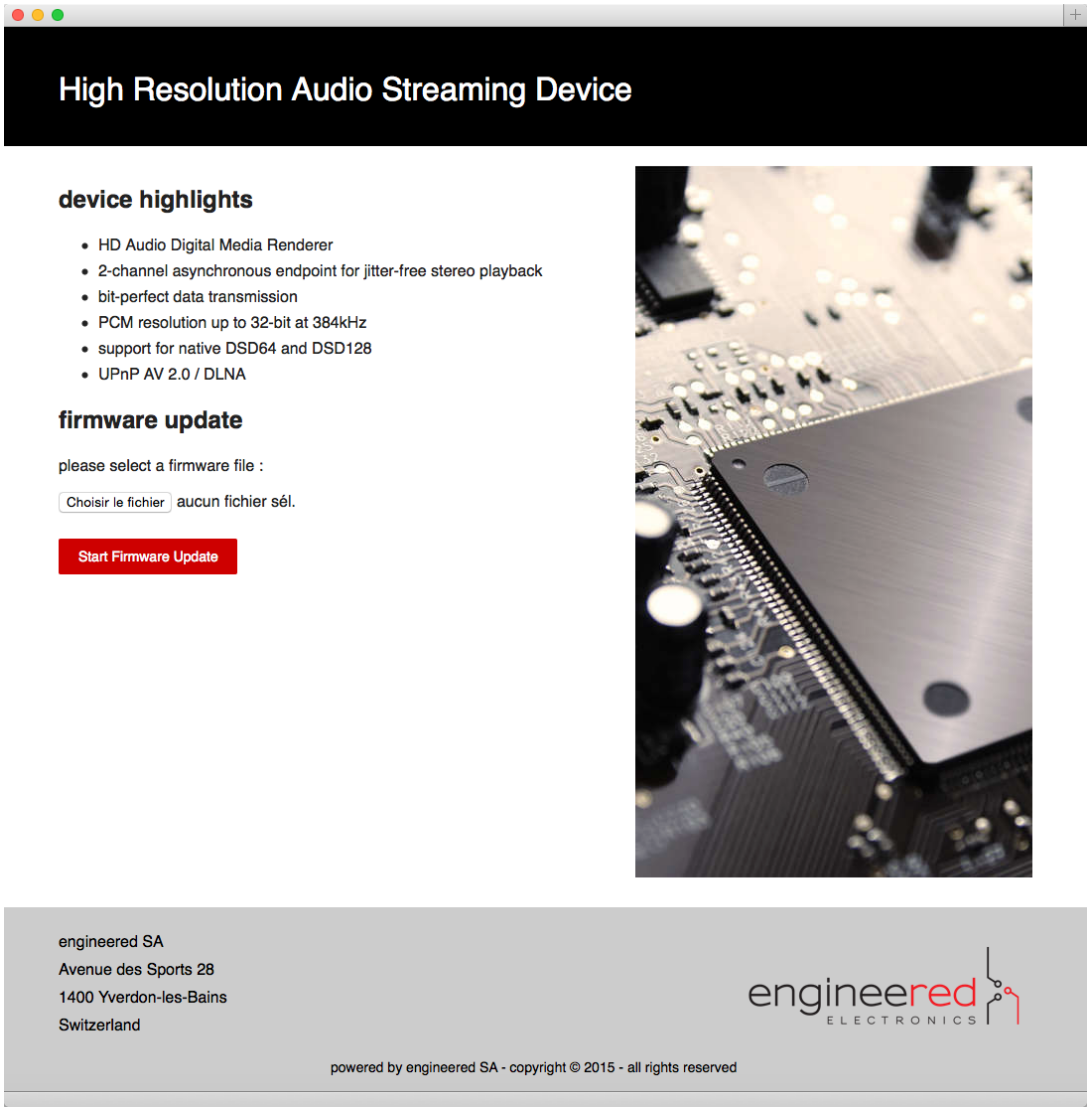

Figure 5-1 – firmware update page

Download the latest firmware on our Web site and save the file on your computer, then extract the ZIP archive. Select the “nmr-abc__vX.XX-...bin” file and click on the “Start Firmware Update” button.

6 Mechanical Data

6.1 Board Dimensions

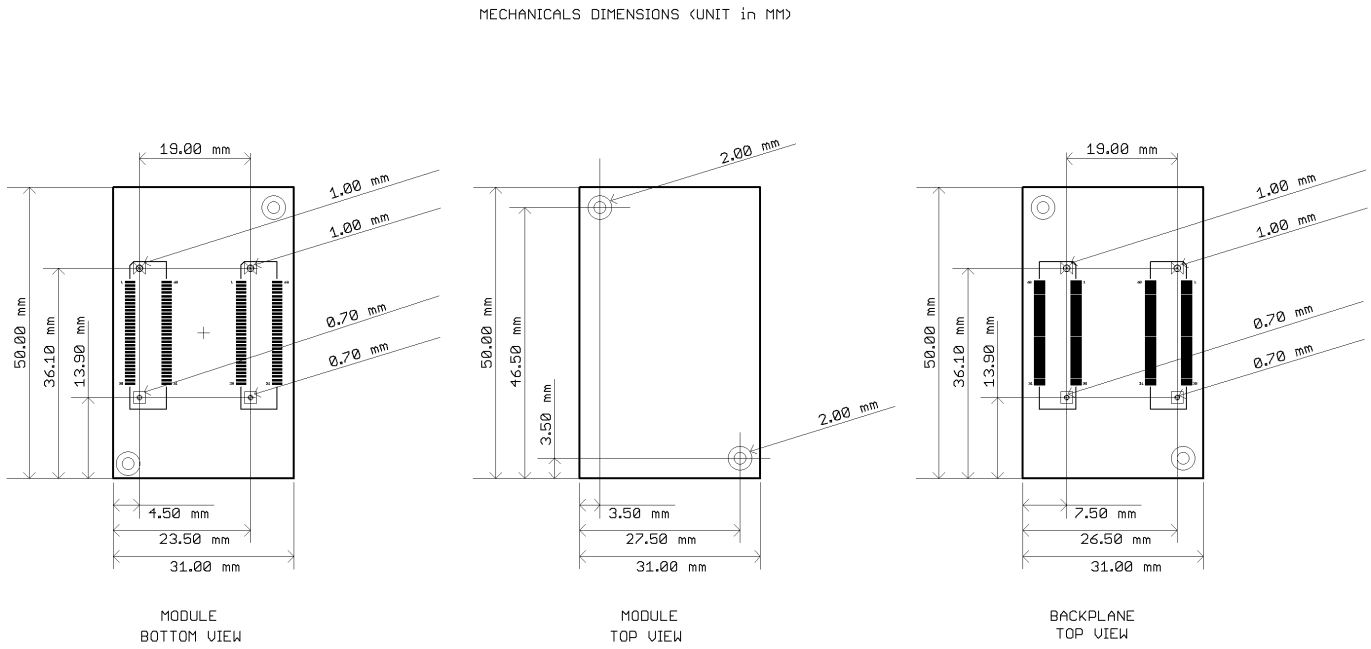

Figure 6-1 – board dimensions

6.2 Module Bottom View

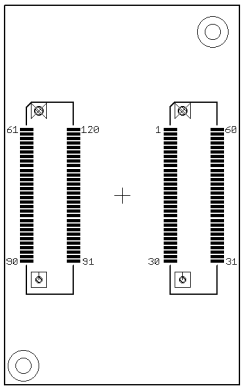

Figure 6-2 – module bottom view

6.3 Module Sides View

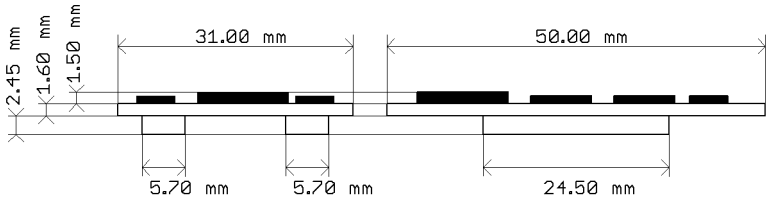

Figure 6-3 – module sides view

6.4 Backplane Footprint Top View

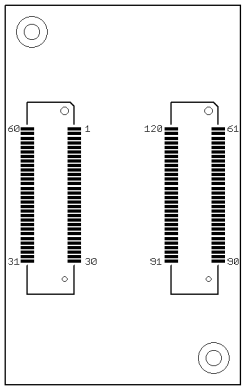

Figure 6-4 – recommended backplane footprint top view

7 Related Products

7.1 Kits and evaluation platforms

engineered offers various solutions to evaluate the MR-MOD streaming technology in full-digital and analog audio environments.

The NMR board is mainly a backplane for the MR-MOD module with on-board clock management and facilitated connexions. It provides digital audio signals on a flex-cable connector as well as buffered and isolated S/PDIF output for easy evaluation.

Please check www.engineered.ch for latest information about evaluation boards availability.

7.2 Custom Applications

The MR-MOD core is based on a modern DSP, which runs engineered's software framework for network-based digital audio playback. This software can be customized on demand for specific requirements.

The NMR hardware platform is mainly foreseen as an evaluation board for engineered's streaming technology. Please check our Web site for more information and contact us for development of custom hardware and software solutions that meets your product requirements.

7.3 S8 and Q8 Upsamplers

The S8 Module integrates four key technologies to deliver a highly integrated asynchronous upsampler and digital synchronizer with best low-level signal linearity and high performance multi-DAC differential output. The module features a single audio input port capable of supporting PCM data up to 384kHz or stereo DSD64 (2.8224MHz) and DSD128 (5.6448MHz). Two digital 8x FS upsampled output ports are available for interfacing to external D/A hardware. It provides highest quality Digital to Analog conversion using two DAC's per channel in differential mode and is a perfect match for the MR-MOD streaming technology in building a High End DAC compatible with latest high definition formats.

The Q8 Module shares the software and hardware technology with the S8 Module, but is optimized for projects requiring a down-sampled output. The first digital audio output port provides up-sampled data at 384kHz for driving a dual-DAC system. The second digital audio output port provides a direct down-sampled stream configurable for 1xFS (48kHz), 2xFS (96kHz) or 4xFS (192kHz) operation.

7.4 DMCK Dual Master Clock Module

The DMCK Module has been developed by engineered in collaboration with an experimented Swiss quartz manufacturer. Thanks to special crystal cut, custom oscillator and clock mux circuits as well as ultimate power supply filtering, the DMCK module provides both 22.5792MHz and 24.5760MHz frequencies with lowest phase-noise figures.

8 Ordering Information

8.1 Part Number

Part Number	Description
MR-MOD	Ethernet Media Renderer Module

8.2 Contact Information

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