XU2S

USB DIGITAL AUDIO INTERFACE

OEM/EVALUATION BOARD DATASHEET

Avenue des Sports 28
1400 Yverdon-les-Bains
Switzerland
+41 21 543 39 66
info@engineered.ch
www.engineered.ch

eR-XU2S-DS
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Preamble

I. About This Datasheet

This document provides the information required for integration and operation of the USB Digital Audio Interface. For more information, please refer to the product description available from the engineered Web site at www.engineered.ch

II. Company Information

engineered SA
Avenue des Sports 28
1400 Yverdon-les-Bains
Switzerland
+41 21 534 39 66
info@engineered.ch
www.engineered.ch

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VI. Documentation Release Notice

This document is under revision control and updates will only be issued as a replacement document with a new version number.

Product specifications are subject to change without notice.

1 Introduction

1.1 Highlights

The USB Digital Audio Interface XU2S is an easy-to-integrate OEM solution for high-end USB audio playback systems, supporting USB Audio Class 2.0. Key features for the eR-XU2S include:

- Based on XMOS xCORE-200 device with an integrated HighSpeed USB 2.0 PHY
- USB Audio Class 2.0 compliant
- 2-channel asynchronous endpoint for highest quality digital audio stereo playback.
- Up to 32-bit resolution, sampling rate up to 384 kHz.
- Support for DSD64 and DSD128 using DoP
- USB Audio Class 2.0 driver available for Microsoft Windows
- Full galvanic isolation
- On-board 22.5792MHz and 24.576MHz ultra low phase noise oscillators.
- Master clock output for DAC synchronization
- I2S/DSD output at CMOS level
- S/PDIF and AES/EBU digital audio outputs, buffered and transformer-coupled

USB streaming is based on an asynchronous protocol, clocked by ultra-low jitter on-board oscillators. Using this concept, the design benefits of a local high quality master clock to achieve highest quality, jitter-free digital audio playback.

Electronic parts have been carefully selected for the best performances. The oscillators have been developed in collaboration with a Swiss clocking devices manufacturer. Special care has been taken for the clock distribution circuit (refer to chapter 3.6 for detailed specifications). All local voltage regulators are very low noise. AES/EBU and S/PDIF transformers are best in class.

Full galvanic isolation avoids any interference issues between the audio device and the USB host. Critical components are powered by an external source to ensure optimal performances. The interface can also be configured to work with bus power only, convenient for using the board as a simple USB to S/PDIF mobile interface. Additionally, connections on USB side are protected against short transient electrostatic discharges.

1.2 USB Considerations

1.2.1 Transmission Mode

There are several different methods for transferring audio data over an USB interface. These methods are:

- Synchronous Mode is a one-way digital connection for transferring data from the PC to the USB device. The computer acts as the clock master for playback and determines the playback timing. Computer and USB timing is not nearly accurate enough for high-fidelity playback.

- Adaptive Mode is another communication method where the computer controls the audio transfer rate. Since the transfer rate is subject to variation, the device clock must adapt to this drifting signal by re-adjusting its own frequency. This approach usually involves a PLL (Phase Locked Loop) and leads to jitter in the derived clock, resulting in compromised sonic performance.

- Asynchronous Mode is a two-way communication method between the computer and the external device. In this case, the device handles the clock and the host is acting as a slave that delivers data according to the rate set by the device.

The eR-XU2S interface is based on the asynchronous mode. Using high speed USB transmission, data are delivered much faster than the playback rate. The on-board DSP manages a memory buffer and controls the USB transmission to make sure that the buffer never gets empty during playback.

Because it eliminates the jitter caused by the PC hardware and software, this concept allows for superior playback performances when compared to other usual audio interfaces.

1.2.2 Compatibility Issues

USB audio devices have stronger requirements for USB hardware and software layers than other USB devices. A faulty hardware component (USB cable or USB port) may have no impact on standard USB devices such as a Flash drive but can be catastrophic for a USB audio device.

Due to the real-time nature of USB audio streams there are also requirements for time characteristic of the operating system and third-party software components installed on the system. Software components that make real-time behavior of the operating system worse are not compatible with audio streaming applications in general.

It is important to note that real-time requirements depend directly on audio latency requirements. If audio latency is not critical (in case of music playback) then timing requirements of the driver are relaxed which increases compatibility with other applications and drivers significantly.

Asynchronous transfer mode uses error checking but no retransmission in case of errors. Electrical noise on USB signals causes errors and thus data loss. This leads to audio signal distortions (clicks). This means that an USB audio device can work only if USB signal quality is good and no error occur. Most other USB device types (Flash drive, printer) are based on bulk transfer mode which uses automatic retransmission in case of errors. These kind of devices are much more tolerant with respect to USB signal distortion.

Quite often the USB cable (or its connectors) is the cause for USB signal distortions. Some cables available on the market are not suited for USB 2.0 high-speed communication (480 Mbps). Also the maximum allowed cable length of 5 meters (16 feet) should not be exceeded.

On some PC main boards (or laptops) signal quality of some USB ports is insufficient for audio streaming. External USB ports (mounted on a front panel or elsewhere in the PC case) are a possible source of USB signal distortion. Quality of cables or connectors used to connect the external USB port with the main board could be insufficient, or internal cables are placed close to the power supply or other sources of electrical noise.

1.3 Audio Formats

The design supports two audio formats, PCM and Direct Stream Digital (DSD).

While Native DSD support is available in Windows though a driver, Apple OS X incorporates a USB driver that only supports PCM. Therefore a method of transporting DSD audio data over PCM frames has been developed, known as DoP (DSD Over PCM). The eR-XU2S Audio design implements the method described in DoP Open Standard 1.1

1.4 DSD Over PCM

Standard DSD has a sample size of 1 bit and a sample rate of 2.8224MHz - this is 64 times the speed of CD. This equates to the same data-rate as a 16-bit PCM stream at 176.4kHz. To clearly identify when this PCM stream contains DSD and when it contains PCM some header bits are added to the sample. A 24-bit PCM stream is therefore used, with the most significant byte being used for a DSD marker (alternating 0x05 and 0xFA values).

When enabled, if USB audio design detects a uninterrupted run of these samples, it switches to DSD mode, using the lower 16-bits as DSD sample data. When this check for DSD headers fails the design falls back to PCM mode. DoP requires bit-perfect transmission - therefore any audio/volume processing will break the stream.

1.5 Functional Block Diagram

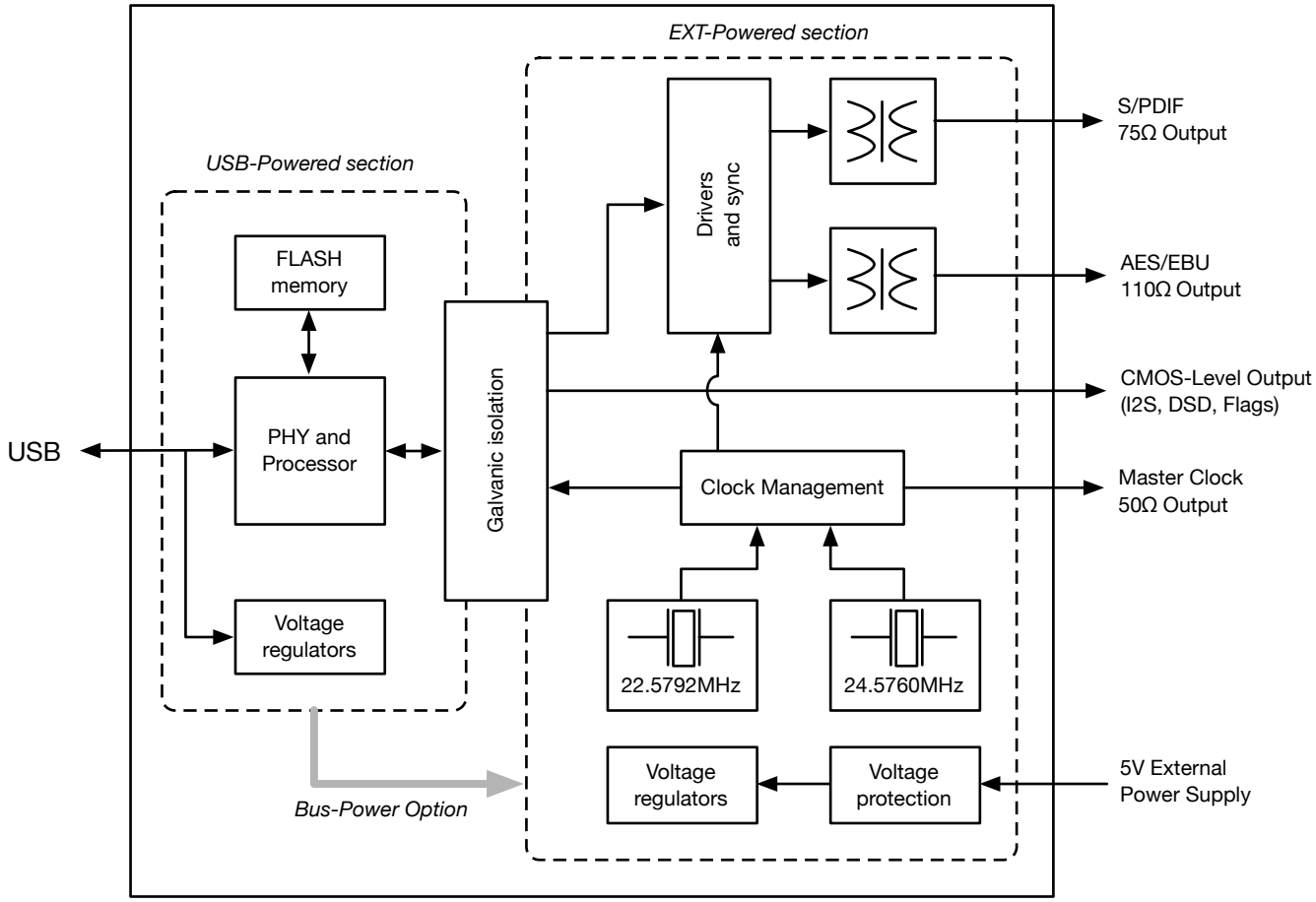

Figure 1-1 – XU2S Functional block diagram

3 Characteristics and Specifications

3.1 Electrostatic Discharge Warning

Many of the components in this product are subject to be damaged by electrostatic discharge (ESD). Customers are advised to observe proper ESD precautions when unpacking and handling the board, including the use of a grounded wrist strap at an approved ESD workstation.

Caution: Failure to observe ESD handling procedures may result in damage to the product.

3.2 Recommended Operating Conditions

Table 3-1 indicates the recommended conditions under which the product should run properly.

Parameter	Recommend Condition
Power supply voltage	5.00 VDC
Operating free-air temperature	$T_{A(min/max)}$: 0 °C / 60 °C

Table 3-1 – Recommended operating conditions

3.3 Absolute Maximum Ratings

The user should be aware of the absolute maximum operating conditions for the eR-XU2S interface. Failure to comply with these conditions may result in damage to the product. The minimum and maximum values are indicated in Table 3-2.

Parameter	Min.	Max.
Power supply voltage	-0.30 V	5.50 V
Input signal voltage	-0.30 V	5.50 V

Table 3-2 – Absolute maximum ratings

3.4 Electrical Specifications

Parameter	Min.	Typ.	Max.	Unit
External DC supply voltage	4.50	5.00	5.50	V
External DC supply current		100		mA
CMOS output high level V_{IH}	2.7	3.10	3.30	V
CMOS output low level V_{IL}	0	0.20	0.40	V
Differential S/PDIF output voltage [output loaded with 75Ω]		0.50		V
S/PDIF output impedance		75		Ω
Differential AES/EBU output voltage [Output loaded with 110Ω]		3.40		V
AES/EBU output impedance		110		Ω

Table 3-3 – Electrical specifications

3.5 Audio Resolution Specification

Parameter	Min.	Typ.	Max.	Unit
PCM digital audio resolution	16		32	bit
PCM digital audio sample rate	32		384	kHz
PCM digital audio dynamic range		32		bit
DSD sample rate	2.8224		5.6448	MHz

Table 3-4 – Audio resolution specifications

3.6 Master Clock Generator Specifications

Specifications here below show typical performances of the complete Master Clock generator circuit, including oscillators, multiplexer and fanout buffer.

Parameter	Min.	Typ.	Max.	Unit
Oscillator frequency stability, all inclusive (temperature, tolerance, aging, supply & load)			+/-50	ppm
Phase noise at 10Hz		-102		dBc/Hz
Phase noise at 100Hz		-132		dBc/Hz
Phase noise at 1kHz		-148		dBc/Hz
Phase noise at 10kHz		-155		dBc/Hz
Phase noise at 100Hz		-158		dBc/Hz

Table 3-5 – Master Clock generator specifications

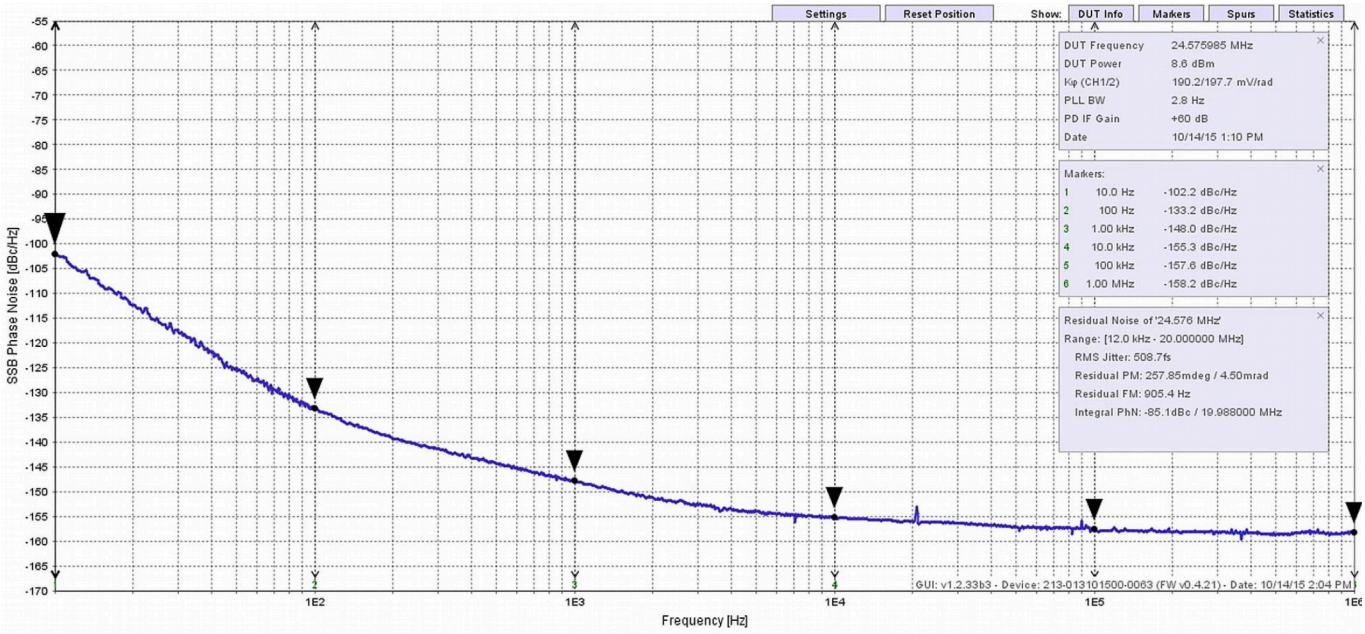

Figure 3-1 - Master Clock generator phase noise plot

4 Connectors Description

Please refer to Figure 6-1 for connectors location on the XU2S board.

4.1 I2S Connector [J7]

Industry standard connector for flat cable, 2.54mm pitch, 20-pos, 3M 2500-series.
Output level: CMOS compliant, refer to Electrical Specifications in chapter 3.4.

Pin #	Name	Type	Description
1	GND	Ground	Ground for I/O and clock management.
2	MCLK	Output	Master Clock Output – Master clock output at 22.5792MHz or 24.576MHz. Refer to Table 5-2.
3	GND	Ground	Ground for I/O and clock management.
4	SPDIF	Output	S/PDIF Output – Serial encoded audio data stream, TTL level.
5	GND	Ground	Ground for I/O and clock management.
6	BCLK	Output	Serial Audio Bit Clock Output – Serial bit clock for PCM and DSD audio data.
7	GND	Ground	Ground for I/O and clock management.
8	PCM_LRCLK /DSDL	Output	Serial Audio Left/Right Clock Output – Frame sync clock for PCM audio data. /Serial Audio Data Output – DSD audio left-channel data.
9	GND	Ground	Ground for I/O and clock management.
10	*reserved*	Output	Reserved for future use.
11	GND	Ground	Ground for I/O and clock management.
12	PCM_SDATA /DSDR	Output	Serial Audio Data Output – Stereo PCM audio data. /Serial Audio Data Output – DSD audio right-channel data.
13	GND	Ground	Ground for I/O and clock management.
14	MUTE#	Output	Mute signal Low: the audio data stream is not valid and the DAC must be muted. High: the audio data stream is valid.
15	DSD_PCM#	Output	Audio Stream Format Low: the digital audio output stream format is PCM High: the digital audio output stream format is DSD
16	44K1_EN#	Output	Sampling Frequency Low: the sampling frequency is a multiple of 44.1kHz. High: the sampling frequency is a multiple of 48kHz. Refer to Table 5-1.
17	RATE0	Output	Sampling Rate – Sampling rate information. Refer to Table 5-1.
18	RATE1	Output	Sampling Rate – Sampling rate information. Refer to Table 5-1.
19	*reserved*	-	Unused. Do not connect.
20	GND	Ground	Ground for I/O and clock management.

Table 4-1 – I2S Connector description

4.2 Master Clock Output Connector [J2]

SMB coaxial male jack, Cinch Connectivity Solutions Johnson ref. 131-3701-261
Suggested matching female receptacle: Cinch Connectivity Solutions Johnson ref. 131-3403-101.
Suggested matching cable: Cinch Connectivity Solutions Johnson ref. 415-0004-006 or 415-0004-012.

Output level: 1.60V typical [50Ω load]
Output Impedance: 50Ω

Pin #	Name	Type	Description
1/Inner	Master Clock	Output	Master Clock Output at 22.5792MHz or 24.5760MHz
2/Outer	GND	Output	Ground

Table 4-2 – Master Clock Output connector description

4.3 S/PDIF Connector [J4]

Vertical Tail Pin Header, 2.54mm pitch, 2-Pos, type Harwin Inc. M20-series

Output level (S/PDIF compliant): 0.50Vpp [75Ω load]
Fully floating, transformer coupled
Output Impedance: 75Ω

Pin #	Name	Type	Description
1	SPDIF pos.	Output	S/PDIF Positive Output – Serial encoded audio data stream, buffered for coaxial cable connection.
2	SPDIF neg.	Output	S/PDIF Negative Output – Serial encoded audio data stream, buffered for coaxial cable connection.

Table 4-3 – S/PDIF connector description

4.4 AES/EBU Connector [J3]

Vertical Tail Pin Header, 2.54mm pitch, 3-Pos, type Harwin Inc. M20-series

Fully floating, transformer coupled
Output level (AES/EBU compliant): 3.40Vpp on 150Ω.

Pin #	Name	Type	Description
1	unsused	-	Unused. Do not connect.
2	AES/EBU pos.	Output	AES/EBU Positive Output – Serial encoded audio data stream, buffered for balanced cable connection.
3	AES/EBU neg.	Output	AES/EBU Negative Output – Serial encoded audio data stream, buffered for balanced cable connection.

Table 4-4 – AES/EBU connector description

4.5 External Power Supply Connector [J5 and J6]

Male Header, horizontal, 2-pos, 3.0mm pitch, Molex Micro-Fit ref. 0436500200
Corresponding box for contacts: Molex 43645-0200

Alternative (parallel connection on Xu2S PCB):
Screw Terminal, 2-pos, 3.81mm pitch, Phoenix Contact 1985823
Corresponding Wire Gauge: 16-30 AWG

Pin #	Name	Type	Description
1	GND	Ground	Electrical ground
2	VDD	Power	Power Supply Input +5.0 VDC.

Table 4-5 – External power supply connector description

Caution: Failure to respect the power supply polarity and voltage level may result in damage to the components.

5 Application Information

5.1 USB Audio Class

The eR-XU2S provides USB 2.0 High Speed device and supports USB Audio Class 2.0.

For operating systems natively supporting USB Audio Class 2.0 specifications such as OS X, the eR-XU2S solution supports driver-free asynchronous playback according to the audio performances specification. A specific USB Audio Class 2.0 driver for MS Windows is available from engineered's Web site.

Note: Bit-perfect digital audio reproduction relies on a correct computer set-up. Audio performances and data integrity highly depends on the OS, media player software and USB audio drivers configuration.

5.2 Master Clock Synchronization

Asynchronous clocking allows for a full control of the USB data transfer and audio master clock to minimize jitter and get the highest digital audio playback quality.

The onboard oscillators and clock management circuit have been designed together with a partner specialized in clocking devices. It is carefully optimized for audio and offers exceptional performances, with an extremely low phase noise in the audio band. Please refer to chapter 3.6 and Figure 3-1 for detailed performance specifications.

For optimal results, we strongly recommend to use the eR-XU2S Master Clock output to drive the Clock Input of the attached D/A converter circuit. Figure 5-1 illustrates a possible eR-XU2S integration with a DAC board.

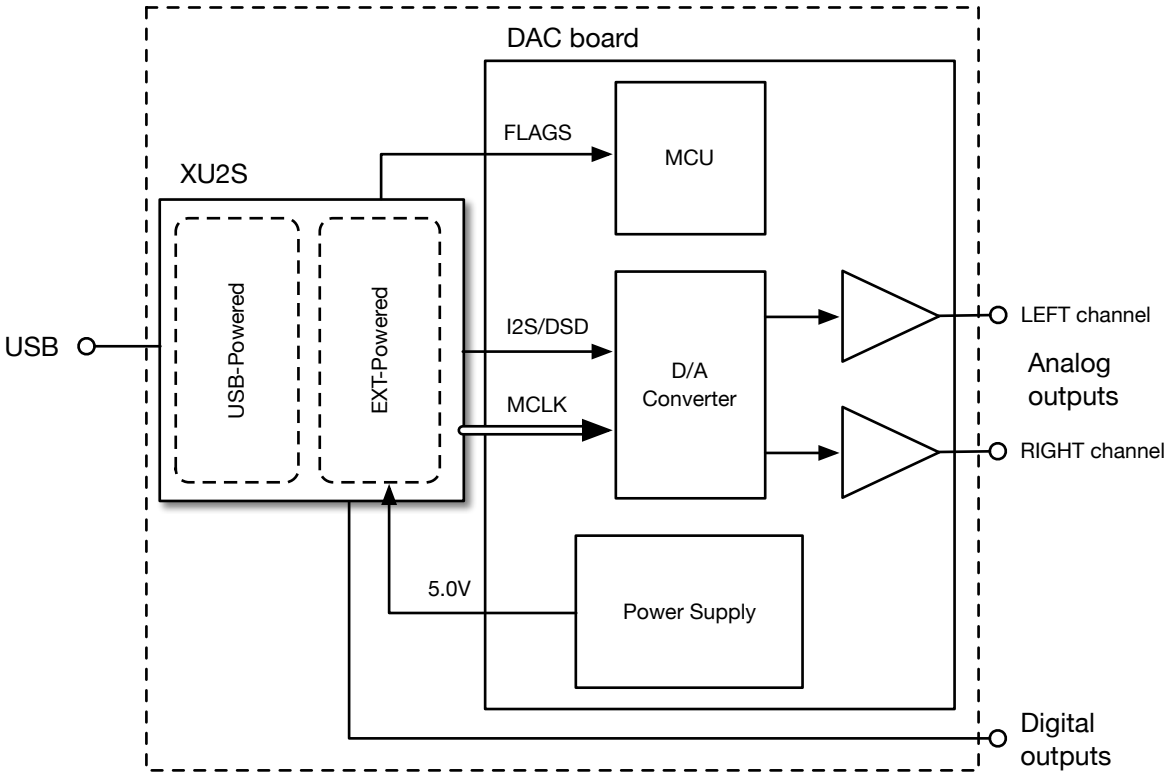

Figure 5-1 - eR-XU2S integration with a DAC board

5.4 Galvanic Isolation

Full galvanic isolation avoids any interference issues between the audio device and the USB host. Critical components are powered by an external source to ensure complete isolation from the host and optimal performances.

The interface can also be configured to use bus power only, useful for using the board as a simple USB to S/PDIF and AES/EBU mobile interface. In this case, all signals on the I2S Connector share the ground reference with the USB input. The S/PDIF and AES/EBU outputs implements dedicated RF transformers thus remaining electrically entirely floating in any case.

Refer to section “Bus-Powered Option” for more information about power supply set-up.

5.5 AES/EBU and S/PDIF Outputs

S/PDIF output is available on the 20-pole connector at standard CMOS level. Additionally, two buffered and isolated outputs for direct coaxial cable connection are provided. Fast drivers coupled to a very high-quality RF transformer ensures signal quality and integrity with standard 75Ω coaxial cables for S/PDIF and 110Ω balanced cabled for AES/EBU.

AES/EBU and S/PDIF standards support PCM up to 192kHz. Higher sampling rate such as 352.8kHz and 384kHz are not supported. For these formats, the I2S digital audio bus on the I2S Connector must be used.

Similarly, DSD cannot be transmitted over S/PDIF. The eR-XU2S decodes DoP and extracts native DSD data for straight connection to a DSD-compatible DAC via the I2S Connector.

5.6 I2S Digital Audio Bus

Both S/PDIF and I2S ports are configured in master mode. The sampling frequency is defined by the USB streaming itself and depends on the audio source file and computer configuration. The PCM sampling frequency is indicated by three flags available on the I2S Connector pin 16 to 18.

Left/Right Clock Frequency (Fs)	RATE0	RATE1	44K1_EN#
44.1 kHz	High	High	Low
48 kHz	High	High	High
88.2 kHz	Low	High	Low
96 kHz	Low	High	High
176.4 kHz	High	Low	Low
192 kHz	High	Low	High
352.8 kHz	Low	Low	Low
384 kHz	Low	Low	High

Table 5-1 – Relation between sampling frequency and hardware flags

Table 5-2 shows how the audio sampling frequency (Fs), the bit clock frequency and the master clock frequency are related.

Left/Right Clock Frequency (Fs)	Bit Clock Ratio	Master Clock Ratio	Master Clock Frequency
44.1 kHz	64 · Fs	512 · Fs	22.5792 MHz
48 kHz	64 · Fs	512 · Fs	24.576 MHz
88.2 kHz	64 · Fs	256 · Fs	22.5792 MHz
96 kHz	64 · Fs	256 · Fs	24.576 MHz
176.4 kHz	64 · Fs	128 · Fs	22.5792 MHz
192 kHz	64 · Fs	128 · Fs	24.576 MHz
352.8 kHz	64 · Fs	64 · Fs	22.5792 MHz
384 kHz	64 · Fs	64 · Fs	24.576 MHz

Table 5-2 – Relation between left/right clock, master clock and bit clock

5.7 DSD mode

Support for DSD64 and DSD128 is provided via DoP open standard in Audio Class 2.0 mode. DSD data format is indicated by the flag DSD_PCM# on I2S Connector pin 15.

DSD_PCM#	Data Stream Type
Low	PCM
High	DSD

Table 5-3 – Data stream type

Table 5-4 shows how the DSD frequency is indicated by the hardware flags, and Table 5-5 illustrates the relation between DSD rate, corresponding sampling rate seen by the USB host in DoP mode, Bit Clock and Master Clock frequencies.

DSD Type	RATE0	RATE1	44K1_EN#
DSD 64	High	High	Low
DSD 128	Low	High	Low

Table 5-4 – Relation between DSD rate and hardware flags

DSD Type	DoP Sampling Rate	Bit Clock Frequency	Master Clock Frequency
DSD 64	176.4kHz	2.8224MHz	22.5792MHz
DSD 128	352.8kHz	5.6448MHz	22.5792MHz

Table 5-5 – Relation between DoP sampling rate, bit clock and master clock

In DSD mode, PCM_LRCLK/DSDL is reconfigured to output Left-channel DSD data. Right-channel DSD data are transmitted over PCM_SDATA/DSDR.

6 Hardware Information

6.1 Connectors and Jumpers Location

The drawing here below shows where the LED's, connectors and jumpers are located on the board.

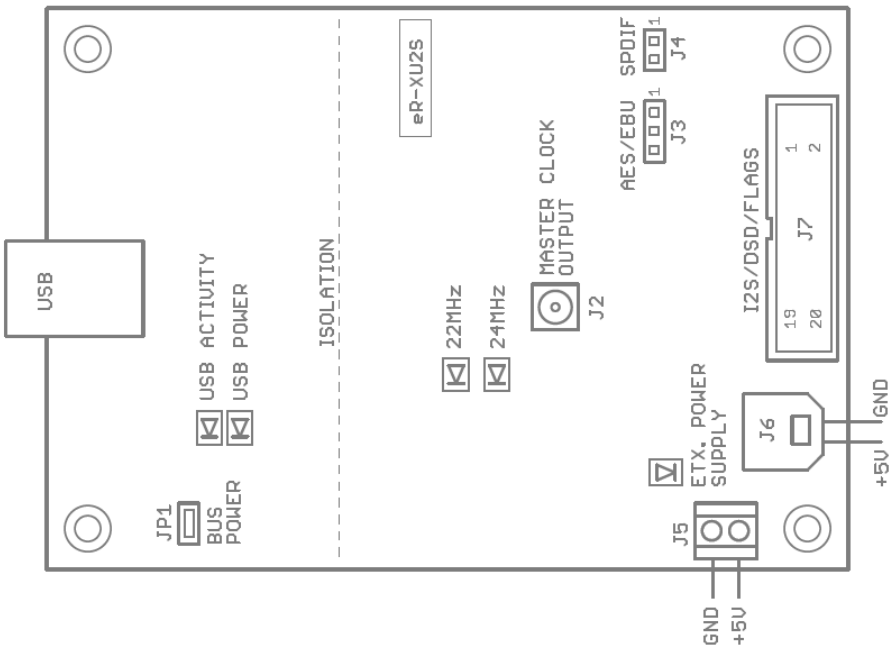

Figure 6-1 – Connectors, LED's and jumpers location

6.2 Bus-Powered Option

Bus-powered option is selected by closing jumper JP1. In this case, there is no galvanic isolation between the USB side and the user application side, all parts are powered by the bus. This set-up is useful for easy testing or using the board as a simple USB to S/PDIF mobile interface.

Caution: External power must never be applied when JP1 is closed.

Leaving JP1 open allows for the use of an external power supply. A 5.0V low noise voltage regulated source is required to ensure optimal performances.

JP1	Power Supply
Open	External
Closed	Bus-powered

Table 6-1 – External power supply selection

6.4 Clock Termination Guidelines

This note is intended to provide basic guidelines necessary to allow end-users to properly interconnect the XU2S Master Clock 50Ω Output to CMOS-input D/A converter chip using SMB connectors. Figure 6-2 shows the basic termination circuit. Components selection is discussed hereafter.

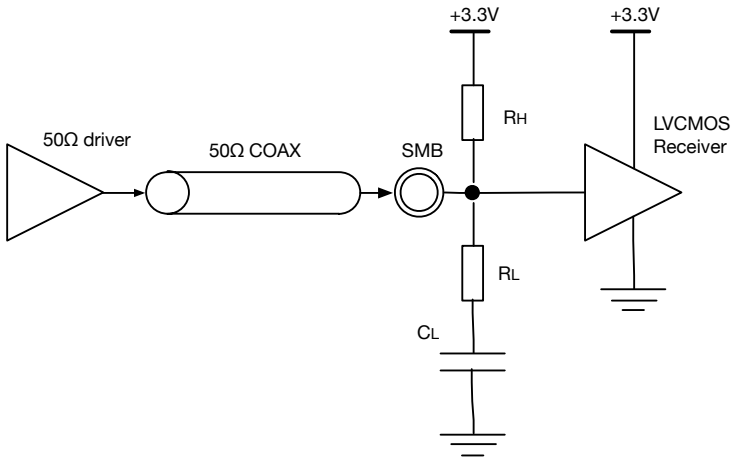

Figure 6-2 – Termination Concept

6.4.1 High Impedance

$R_H = R_L = \infty$

This Source Termination method is a very common way for single receiver, point-to-point situation. Although this works with standard LVCMOS inputs, it is not the best option regarding signal integrity and jitter.

6.4.2 50Ω Termination

The equivalent impedance is given by R_H and R_L in parallel, such as R_H and R_L form a 50Ω impedance. From signal integrity point of view, this is the traditional way to do it. We can consider 2 options:

a) $R_L = 50\Omega$, $R_H = \infty$
With C_L shorted, the clock signal amplitude at the receiver input stays between 0V and VDD/2. This situation is not compatible with usual LVCMOS inputs.

Adding C_L helps as the signal is now centered on VDD/2. However, if the driver goes into high-impedance, the receiver input is floating.

b) $R_L = 100\Omega$, $R_H = 100\Omega$
With C_L shorted, the clock signal amplitude at the receiver input is between 0.25VDD and 0.75VDD. This situation is optimal if the receiver switching levels are 30% and 70%.

The receiver input is at VCC/2 if the driver goes into high-impedance (CMOS input gates draw more current in this case). Adding C_L solves this issue by pulling the line to VDD in driver OFF state, but the active signal is then shifted between 0.40VDD and 0.90VDD which may be again not compatible with LVCMOS inputs.

In the above circuit options, capacitor C_L shall be calculated so that its impedance at the operating frequency is less than 5Ω.

6.5 Board Dimensions

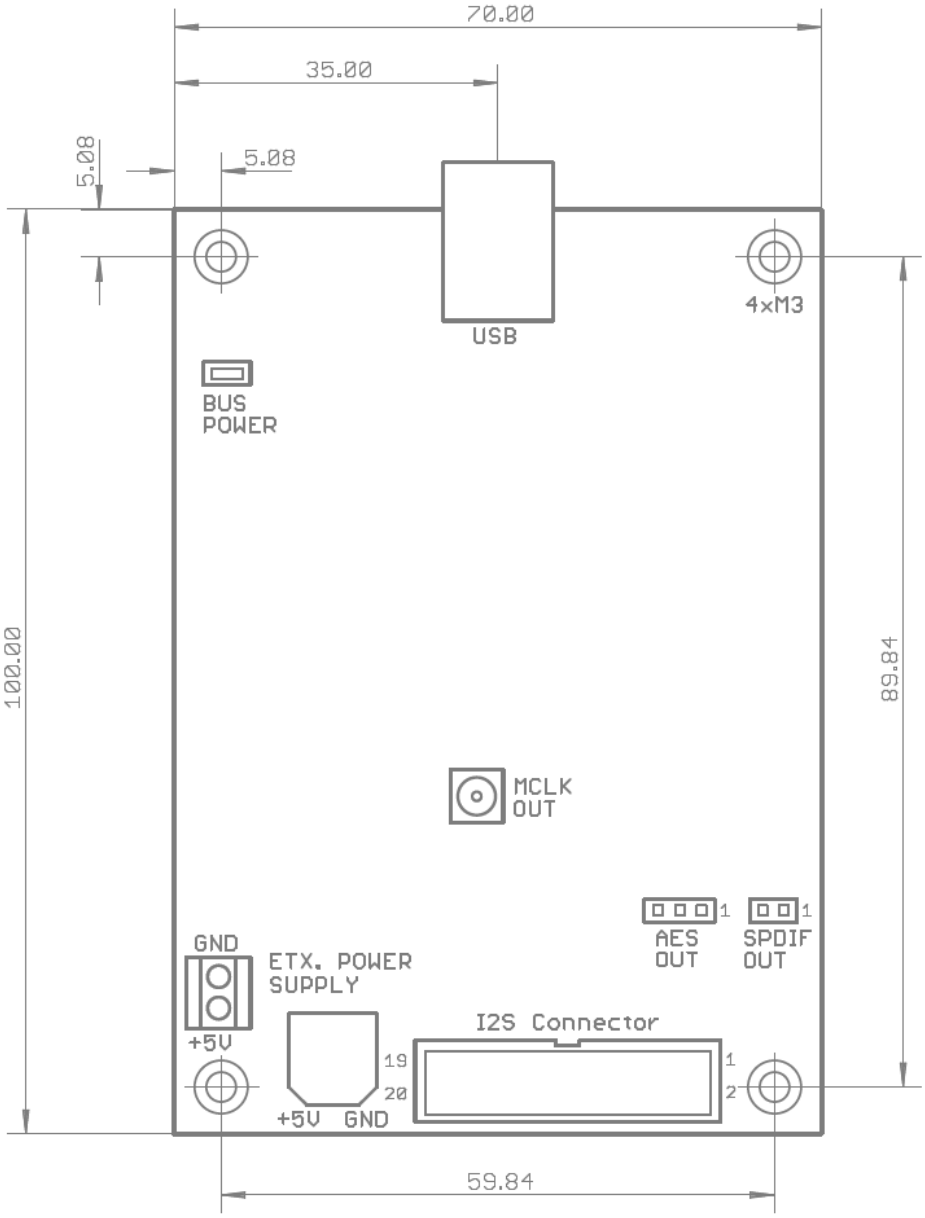

Figure 6-3 – Mechanical dimensions in millimeters

7 Ordering Information

7.1 Part Number

Part Number	Description
eR-XU2S	XU2S USB Digital Audio Playback Interface